Current-fed Quasi Z-Source Inverter with FPGA Application of Digital Controller

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Abstract— This paper presents, FPGA application of fully digital controller for three-phase quasi z-source inverter (qZSI) with switching strategies contain boost control and buck control. The Field Programmable Gate Arrays (FPGAs) have present high computational capacity and adjustability due to their parallel execution and reconfigurable hardware. In this technique blocks are based on expected digital circuits only with combinational logic and using pipelining technique. The proposed digit controllers have been successfully synthesized and application by Quartus II 9.1V and Cyclone II FPGA, to destination device EP2C20F484C6. Fulfilled result demonstrates that the proposed technique has features containing reconfigurable, low-cost, high speed and also it is very perfect.

Keywords: *qZSI, Field Programmable Gate Arrays, FPGA.*

I. INTRODUCTION

The purpose of an inverter is to change a DC input voltage to an AC output voltage of preferred frequency and magnitude. Output voltage may be fixed or changing at a fixed or changing frequency. Changing output voltages are achieved by change the input DC voltage with maintaining the inverter gain. At same time, if the DC input voltage fixed and not controllable, changing output voltage can be achieved by fixing the modulation index which is normally done by implementing Pulse Width Modulation (PWM) control within the inverter [1].The quasi z-source inverter (qZSI) provides special features which can be realized in the traditional Voltage Source Inverter (VSI) and current source inverter (CSI).

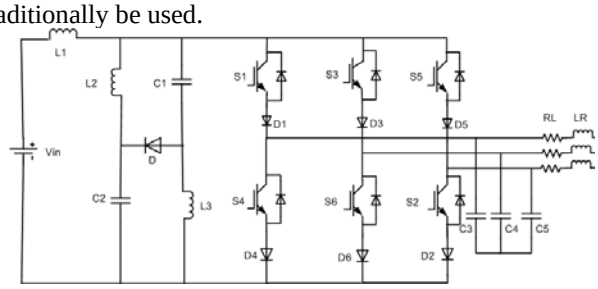
- The quasi Z-source inverter is a boost converter for dc as power changing and greater peak to peak ac output voltage can be realized than obtainable input voltage.
- The main circuit of voltage source converter and current source inverter cannot be interchangeable.
- The cross conductive short circuit is called shoot through state and is same to those in Current Source Inverter.
- Shorting of any phase legs provides a boost up aptitude thus must be carefully controlled.

The inverter controllers are admitted PWM, modified SPWM, space vector PWM (SVPWM) and PWM proportional quasi Z-source inverter (boost, buck). These modes are established with two basic technologies according to control method. The first technology is depend on devices contain microcontrollers and DSP (Digital Signal Processor) with software control techniques, this group are established with high level language (C, C++, ...) and PWM signals and timers of microcontrollers and DSPs, thus this mode is based on devices and provides a quick low-cost manufacturing solution for only special applications. But the for high-frequency switching power devices, with complex modulation schemes it is unsuitable. The control method is SVPWM that archetype of converters are built using DSP. The FPGA consist thousands of logic gates, some of which are array together as a configurable logic block (CLB) to facilitate higher level circuit design. The beneficiary of FPGA technology has enabled acrid archetype of digital systems. But, with the advance of high-frequency switching power devices, complex modulation schemes can no longer be attained. If use to FPGA for PWM strategies provides advantages such as acrid archetype, simple hardware and software design, higher switching frequency, and acquit the computation load of microprocessors.

II. CURRENT-FED QZSI CIRCUIT ANALYSIS

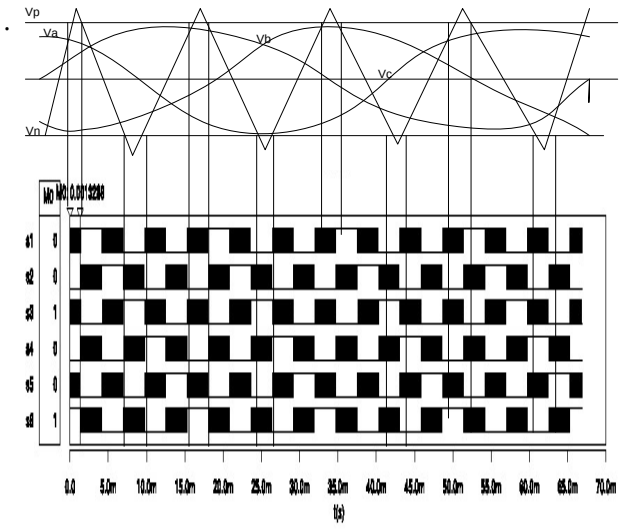
The quasi-Z-source inverters (qZSIs) were recently proposed as an important improvement to the traditional Z-source inverters (ZSIs). Mainly the previous works on quasi Z-source inverter: Current-fed Quasi-Z-Source Inverter with Coupled Inductors [1], Current-fed quasi-Z-source inverter with voltage buck-boost and regeneration capability [2], Discontinuous operation modes of current-fed Quasi-Z-Source inverter [3]. QZSI have been redacted which appearance several advancements and no disadvantages when compared to the traditional ZSIs. They are voltage-fed qZSI with continuous and discontinuous input current and current-fed qZSI with discontinuous input current. The current-fed quasi Z-source inverter in a method resemble with the current fed ZSI, are bidirectional with the diode, D. The quasi Z-source inverter shown in Fig.1, appearance abate current in inductor L_1, as well as abate passive component count and appearance lower current in inductors L_2 and L_3. quasi Z-source inverter in Fig.1 do not need input capacitance. All four quasi Z-source inverter topologies also appearance a common dc rail between the source and inverter, unlike the traditional ZSI circuits. Supplementary, these quasi Z-source inverter circuits have no disadvantages when compared to the traditional Z-source inverter topologies. These quasi Z-source

inverter topologies therefore can be used in any application in which the Z-source inverter would traditionally be used.



III SIMPLE BOOST CONTROL METHOD

The best method for control and switching of current-fed qZSI is pulse width modulations. As detailed in [4], two PWM control methods, termed as the simple boost control method and the maximum boost control method has been investigated, which result in the different associations of the voltage boost inversion's capacity versus the given modulation index M, because the above-mentioned two methods can be observed as the theoretical basis of diverse advanced PWM approaches such as the harmonic injection method and the space vector PWM method. It is seen in Fig. 2 that in the simple boost control, a straight line equal to or greater than the peak value of the three phase accreditation is active. The derivable duty ratio of the traditional state can be regarded as a constant value, and its maximum value is limited to (1−M). As seen in Fig. 2 two straight lines V_p and V_n purpose amount of surface pulse the traditional state. If the carrier (triangular waveform) greater of the V_p traditional zero is collect place and also if carrier less of the V_n traditional zero is collected place



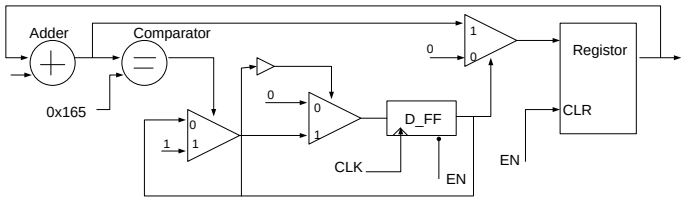
3.1.1 Proposed operation of Simple Boost Control on FPGA

The FPGA is standard integrated circuits that can be programmed by a user to ability a array of complex logic functions. The FPGA has the efficiency of being reconfigurable within a system, which can be a big advantage in applications in the switching operation. Logic circuits are designed by the programmer in a software (two common languages for FPGA design are called VHDL and Verilog), then moved into the FPGA chip [2]. This proposed method is including three parts:

1. produce sinusoidal signal
2. produce a triangular waveform
3. Pulse produce module

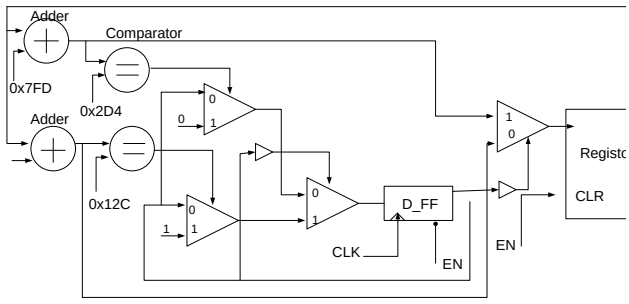
1. Produce Sinusoidal Signal and produce Strategy

In order to produce 50Hz sinusoidal signal we obtain 360 points of each 220sin(x), 220sin(x+120) and 220sin(x-120) and put every one of 360 points in symmetrical Look up Table (LUT). So by each rising edge of the clock signal one of the samples of the sine wave is moved to the output. LUTs are concurrent with the rising edge clock signal thus depending on good continuity in giving sinusoidal waveform and we have a continuous waveform absolutely. In other hand, in difference stage triangular waveform and sinusoidal signals these operations are executed on all samples in each rising edge of the clock signal, so the observation is concurrent with the clock and accuracy control method is very good. The input of LUT really is the same line addressing memory part sinusoidal waveform samples saved in the LUT. Input lines of address are design by the address produce module. Proposed address produce module product address of x"000" to x"168" that equal 0 to 360 points of sine waveform. As shown in Fig. 3, the proposed address produce module first product address x"000" with each rising edge of the clock address produce is incremented one unit until address value equal with x"168" one more time state of address produce is change in x"000". Schematic of proposed address produce module is shown in Fig. 3. As seen in Fig. 3 with each rising edge of the clock adder is increment one unit, amount of output adder is addressed and transfer to the output register. One comparator is used for analyze the last address (0x168) with output adder, if the last address observe output of D Flip-Flop is „0" so output register equal to zero, again address produce start with x"001" this cycle is reproduced again.



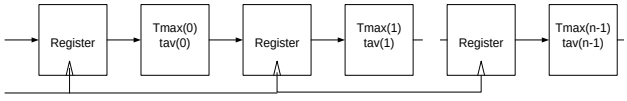
3.1.1.2Produce Triangular Waveform

In order for the application of triangular waveform produce module use a counter with two modes, add negative number and positive number. One multiplexer is the use for switch among these modes. In this proposed circuit first mode is "0" counter start of "0" to a greater number (for example 300) then the mode is "1" and counting to smallest number (for example -300) again mode is "0" ,thus triangular waveform is produced. Proposed digital design schematic is shown in Fig. 4 output D flip-flop is mode signal. In this circuit two comparators are used in proposed digital design one for comparing counter with greater number and another for comparing counter with less number and also two adders are used in proposed digital design that one of adders is for add one unit in mode "0" and another is for less one unit in mode"1".



3.1.1.3 Pulse Generation Module

This block create of three comparators so that with each rising edge of the clock one of the comparators analyze one sample of the 50Hz sinusoidal waveform with one sample of 10KHz triangular waveform. If sample of 50 Hz sinusoidal waveform is bigger than sample of 10 KHz triangular waveform PWM_a output signal be "1" and PWM_na be "0" so that PWM_a is not PWM_na. Other comparators are for comparing V_n and V_P with samples of a triangular waveform if the triangular waveform is largest than V_p traditional zero state is taking place also if triangular waveform be less than V_n traditional zero state is taking place. One of the advantage proposed circuit is totally of the sample triangular Waveform is analyzed with V_{an} and V_P and all sample don't lose in comparison, thus comparison operation done completely because this circuit is proportion with a clock signal. The PWM pulse is produced exactly. We increment speed by pipelining technique in proposed digital circuit. Pipelining is an application technique in which multiple data are overlapped in execution, also pipelining creating digital designs fast. There is interest in pipelining when the next data can action the following clock cycle. As a universal example in [35]. look at the pipelined circuit. For each block, for example number i, are identify a max delay $t_{max}(i)$ and an average one $t_{av}(i)$. The Esotericism and through put of the circuit of Fig. 5 are equal to n. $T_{clk.}$

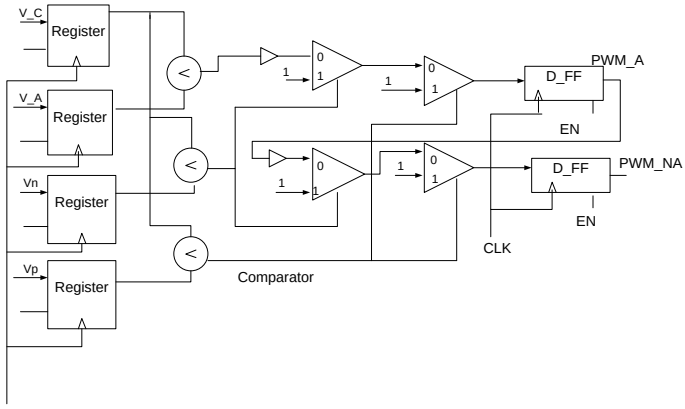


And $1/T_{clk}$, appropriately where $T_{clk} > \max\{ t_{max}(0), t_{max}(1), \dots, t_{max}(n-1)\}$, that is,

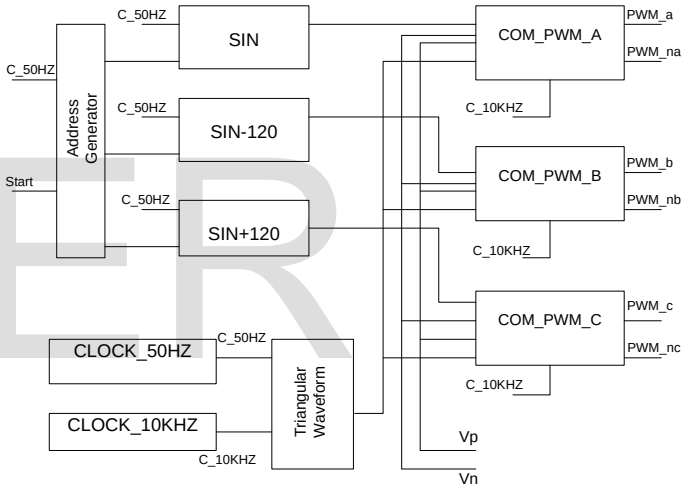
Esotericism $> n.\max\{ t_{max}(0), t_{max}(1), \dots, t_{max}(n-1)\}$,

all through $< i/\max\{ t_{max}(0), t_{max}(1),\dots, t_{max}(n-1)\}$.

In this architecture we apply pipelining technique by registers and two D Flip-Flops. Fig. 6 shows proposed digital architecture for only signals PWM_a, for PWM_b and PWM_c digital circuit is same.



As seen in Fig. 6, four inputs V_C, V_A, Vn and, V_P are obtaining with each rising edge of the clock. We use three comparators, one comparator for analyzing samples of a triangular waveform (V_C) with samples of sinusoidal waveform (V_A), another for analyzing triangular waveform (V_C) with the v_{an} and also a last comparator for analyzing triangular waveform (V_C) with Vp. Multiplexers symmetrical output comparators determine "0" or "1" be signals PWM_a and PWM_na.



IV. Comparison and Simulation

We conception a novel optimized and high achievement fully digital controller on FPGA for switching control three phases quasi ZSI. The suggested method has best achievement hardware and software than conventional methods. The suggested method has been written with VHDL (hardware description language). In procedure to get certain numbers for the hardware usage thus this work was synthesized and achieved using Quartus II 9.1V software, cyclone II FPGA to target device EP2C20F484C6. Also for the evidence of the proposed method, we do simulation result . The Fig. 11 and Fig. 12 shows waveform result of suggested digital design for simple boost control.

V. Conclusion

The aim of this paper is to develop and implement an FPGA based fully digital controller for ZSI with simple boost control and maximum boost control. The simulation results ensure the feasibility of the high-speed FPGA architecture of the novel proposed digital controller. The advantages of this technique over the others available in the literature include flexibility, high accuracy and reduced area. We first design proposed method based on the fully digital circuit, then implement in FPGA. In this paper, mainly we design and application

of the digital modified pulse width modulation based on proposed digital circuits for switching control in three phase z-source inverter

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